ABSTRACT OF THE DISCLOSURE

The present invention discloses a mask ROM which has excellent compatibility with a logic process and improves integration of a memory cell, and a fabrication method thereof. The mask ROM includes: a substrate where a memory cell array region and a segment select region are defined; first and second trenches respectively formed at the outer portion of the memory cell array region and at the outer portion of a buried layer formation region of the segment select region; an element isolating film and an isolating pattern respectively filling up the first and second trenches; a plurality of buried layers aligned on the substrate in a first direction by a predetermined interval, and surrounded by the isolating pattern; and a plurality of gates aligned in a second direction to cross the buried layers in an orthogonal direction.